REMARKS / ARGUMENTS

Claims 1-49 are pending in the instant application, of which claims 3 and 22-24 have been cancelled, and claims 42-49 are new claims. Claims 1, 18, 26, 33, 36 and 39 are independent. Claims 2, 4-17, 42-45, 19-21, 25, 27-32, 46-49, 34-35, 37-38 and 40-41, depend directly or indirectly from independent claims 1, 18, 26, 33, 36 and 39, respectively.

Claims 1-2, 4-21, 25-27, 28-37 and 39-40 have been amended to clarify the claim language. The Applicant points out that support for the above listed claim amendments and new claims may be found at least in paragraphs [0014]-[0016], [0033]-[0040] and in Figs. 6, 7 and 9.

Claims 18, 20, 22-29, 31, 32 and 36-41 are rejected under 35 USC 102(e) as anticipated by Philbrick et al. (US Pub. No. 2001/0037406, hereinafter Philbrick).

Claims 1-15 are rejected under 35 USC 103(a) as being unpatentable over Applicant's Admitted Prior Art (background of the invention and FIG. 1-5, hereinafter AAPA), and further in view of Philbrick.

Claims 33-35, 30 are rejected under 35 USC 103(a) as being unpatentable over Philbrick as applied to claim 26 above, and further in view of Microsoft (Winsock Direct and Protocol Offload on SANs, 03/03/2001).

Claims 16-17 are rejected under 35 USC 103(a) as being unpatentable over AAPA-Philbrick, as applied to claims 1 and 14 above, and further in view of Microsoft.

Claims 19 and 21 are rejected under 35 USC 103(a) as being unpatentable over Philbrick, in view of what has been known in the art.

The Applicant submits that the claims 1-2, 4-21 and 25-49 define patentable subject matter in view of the following remarks and arguments.

I. Examiner's Response to Arguments in the Final Office Action

The Examiner in page 2 of the Final Office Action disagrees with the Applicant that Philbrick in claim 18 does not teach "a single Ethernet connector ... concurrently handle a plurality of different types of traffic." The Examiner relies for support on Philbrick in Fig. 6, and ¶0065 lines 15-17 and argues that Philbrick's MAC controller 424 is an alleged single L2 SAN connector. The Applicant respectfully disagrees, and points out that even with the broadest interpretation, Philbrick's "MAC controller 424 still cannot be equated to be the same as the claimed "Ethernet connector", or vice versa.

Specifically, the Applicant points out that an "Ethernet connector" is merely a passive mechanical hardware for interfacing IEEE 802.x specifications network signals. The claimed "Ethernet connector" does not utilize active electronic hardware such as IC and program codes to perform signal processing functions, which Philbrick's MAC

controller 424 does. In this regard, the Examiner is erroneous in equating Philbrick's MAC controller 424 to the claimed "Ethernet connector" as recited in claim 18.

Assuming arguendo that Philbrick's MAC controller 424 is the alleged "Ethernet connector," which the Applicant respectfully asserts it is not, the Examiner's next assertion that the iSCSI PDUs can be considered as two independent and distinct network traffic types is unsupported by Satran's internet Draft Document: draft-ietf-ips-iscsi-07.txt (hereinafter referred as "Satran"). The Examiner seems to base his argument by referring to the iSCSI PDU de-encapsulation process, where the iSCSI PDU the header is being processed by the various protocol processors, including Philbrick's processor 408 or by the HBA controller in the storage network devices. The Examiner seems to allege that Satran teaches that the iSCSI protocol are in fact two separate protocols, namely the TCP/IP protocol (the alleged second traffic type), and the SCSI protocol (the alleged first traffic type).

The Applicant respectfully disagrees and refers the Examiner to the disclosure of iSCSI by Satran, which is incorporated by reference in Philrbick's ¶0065. Specifically, Satran in section 1.2 discloses that "the **iSCSI protocol is a mapping** of the **SCSI remote procedure invocation model over the TCP protocol**." In the same section, Satran also teaches such iSCSI communication protocol is sent in the form of a communication message, referred to the term "iSCSI protocol data unit" (iSCSI PDU). In other words, Satran clearly teaches that the iSCSI is a protocol that maps the SCSI protocol over the TCP protocol, and such protocol is communicated through a message

type, which is also known as a **iSCSI PDU message**. Therefore, the Examiner's argument that the iSCSI PDU has two separate and distinct network traffics is contrary to the disclosure of Satran.

Furthermore, the Applicant points out the Examiner seems to ignore the fact that the processing of the iSCSI PDU messages headers (i.e., the de-encapsulation process) by various processors takes place only after the iSCSI PDUs has been transported via the network link, the fabric and received by the Ethernet connector . In other words, the iSCSI PDU messages are still considered as a single traffic type, having a single connection source and destination address before being processed.

Based on the above rationale, the Applicant maintains the argument in the July 24, 2008 reply to the Office Action, that the iSCSI traffic is of a single traffic type, and not two separate types. Therefore, Philbrick does not disclose or suggest the claimed "a single Ethernet connector **for handling a plurality of different types of network traffic transported via the single fabric**," as recited in the Applicant's claim 18.

In addition, regarding the rejection to claim 18, the Applicant submits that Philbrick does not disclose or suggest "a **single integrated convergent controller chip** ... operable to **concurrently handle a plurality of different types of traffic**," as recited by the Applicant in claim 18. The Examiner alleges that Philbrick's processor 408 is a single integrated chip, but the Applicant points out that Philbrick does not disclose that the processor 408 is an "integrated convergent controller chip".

Specifically, the Examiner is referred to Philbrick in Fig. 16, where Philbrick discloses separate controllers. Philbrick discloses that there are four MAC controllers 722-728 for processing L2 level protocols of four incoming network traffics, a separate SRAM and DMA controller 740 for DMA function, a separate microprocessor 780 for processing packet headers to decide fast path or slow path traffics, and a host CPU 30 (see Philbrick in Fig. 6) for processing the slow path packets in the protocol stack 38. In this regard, Philbrick uses separate controllers in the INIC, and in the host 20 to carry out separate protocol and controller functions. Philbrick simply does not disclose or suggest "a **single integrated convergent controller chip** ... operable to **concurrently handle a plurality of different types of traffic**," as recited by the Applicant in claim 18.

Furthermore, regarding the rejection of claim 18, the Applicant further submits that Philbrick does not disclose or suggest "a single Ethernet connector for handling a plurality of different types of network traffic transported via a single fabric, ...**the single fabric is coupled to a plurality of servers**," as recited by the Applicant in claim 18. The Examiner equates Philbrick's single wire connecting between the MAC 424 and the processor 408 inside the INIC 400 to the claimed "single fabric". The Applicant respectfully disagrees, and points out that not only the MAC 424 is not a "single **Ethernet connector**", but also Philbrick discloses that the alleged single fabric (single wire) **connects between the MAC 424 and the processor 408 inside the INIC 400**, therefore, Philbrick's alleged single fabric does not read on "**the single fabric is coupled to a plurality of servers**," as recited by the Applicant in claim 18.

Therefore, based on the foregoing rationale, the Applicant respectfully maintains that Philbrick does not anticipate the Applicant's limitation of "a **single integrated convergent network controller chip**, and a **single Ethernet connector for handling a plurality of different types of network traffic transported via a single fabric,** said single Ethernet connector is coupled to **the single integrated convergent network controller chip ... operable to concurrently handle a plurality of different types of traffic,... the single fabric is coupled to a plurality of servers**" as recited by the Applicant in claim 18. Claim 18 should therefore be allowable based on the above rationale.

Likewise, independent claims 1, 26, 33, 36 and 39 are similar in many respects to claim 18, are also submitted to be allowable based on the same rationale of claim 18.

II. REJECTION UNDER 35 U.S.C. § 102

MPEP 2131 states:

> "[a] claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *See* MPEP at 2131 (internal citation omitted). Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See id.* (internal citation omitted).

A. Philbrick Does Not Anticipate Claims 18, 20, 22-29, 31, 32 and 36-41

The Applicant turns to the rejection of claims 18, 20, 22-29, 31-32 and 36-41 under 35 U.S.C. § 102(e) as being anticipated by Philbrick. Without conceding that Philbrick qualifies as prior art under 35 U.S.C. 102(e), the Applicant respectfully traverses this rejection as follows.

A(1) Independent Claims 18, 26, 36 and 39

With regard to the rejection of independent claim 18 under 35 U.S.C. § 102(e), the Applicant submits that Philbrick does not disclose or suggest at least the limitation of "a **single integrated convergent network controller chip** ... operable to **concurrently handle a plurality of different types of traffic**," as recited by the Applicant in claim 18.

At page 4 of the Final Office Action, the Examiner relies for support on Fig. 6 of Philbrick and alleges that the processor 408 is an integrated chip. The Applicant points out that despite that the processor 408 is an integrated chip, Philbrick does not disclose or suggest that the processor 408 is the claimed "**single integrated convergent network controller** chip".

The Examiner is referred to the above Examiner's Response to Arguments in the Final Office Action argument in section I, that Philbrick in Fig. 16, discloses separate controllers. Specifically, Philbrick discloses that there are four MAC controllers 722-728 for processing L2 level protocols of four incoming network traffics, a separate SRAM

and DMA controller 740 for DMA function, a separate microprocessor 780 for processing packet headers to decide fast path or slow path traffics, and a host CPU 30 (see Philbrick in Fig. 6) for processing the slow path packets in the protocol stack 38. In this regard, Philbrick uses separate controllers in the INIC, and in the host 20 to carry out separate protocol and controller functions. Philbrick simply does not disclose or suggest "a **single integrated convergent network controller chip** ... operable to **concurrently handle a plurality of different types of traffic**," as recited by the Applicant in claim 18.

In addition, with regard to the rejection of claim 1, the Applicant submits that Philbrick does not disclose or suggest at least the limitation of "a single Ethernet connector for handling a plurality of different types of network traffic transported via a single fabric," as recited in Applicant's claim 18. In the Final Office Action, the Examiner asserts that Philbrick discloses the following:

> "an Ethernet connector coupled to the integrated chip ([0066] lines 12-15, Ethernet connector 424 which is a MAC controller)" wherein the Ethernet connector and the integrated chip can handle a plurality of different types of traffic ([0065] lines 15-21, iSCSI and TCP/IP)."

See the Final Office Action, page 4. The Examiner in the Examiner's response to argument at page 2 of the Final Office Action equates Philbrick's MAC controller 424 to an alleged single L2 SAN connector. The Applicant respectfully disagrees, and refers the Examiner to the above argument in section I, and points out that even with the

broadest interpretation, Philbrick's "MAC controller 424 still cannot be equated to be the same as the claimed "Ethernet connector", or vice versa.

Specifically, the Applicant points out that an "Ethernet connector" is merely a passive mechanical hardware for interfacing IEEE 802.x specifications network signals. The claimed "Ethernet connector" does not utilize active electronic hardware such as IC and program codes to perform signal processing functions, which Philbrick's MAC controller 424 does. In this regard, the Examiner is erroneous in equating Philbrick's MAC controller 424 to the claimed "Ethernet connector" as recited in claim 18.

In addition, the Examiner seems to allege that the iSCSI traffic type is not a single traffic type, but instead are two traffic types, i.e., the SCSI storage as the first traffic type, over the internet TCP/IP network traffic as the second traffic type. The Examiner relies for support on the following citation of Philbrick:

> "SANS 418 and 420 may run a storage protocol such as SCSI over TCP/IP or SCSI Encapsulation Protocol (SEP). One such Protocol is described by Satran...entitled iSCSI..."

See Philbrick at ¶[0065], lines 15-21. The Applicant refers the Examiner to the same argument in Section I above, and respectfully disagrees with the Examiner's interpretation that there are two traffic types within the iSCSI traffic type.

Assuming arguendo that Philbrick's MAC controller 424 is the alleged "Ethernet connector," which the Applicant respectfully asserts it is not, the Examiner's next assertion that the iSCSI PDUs can be considered as two independent and distinct network traffic types is unsupported by Satran's internet Draft Document: draft-ietf-ips-

iscsi-07.txt (hereinafter referred as "Satran"). The Examiner seems to base his argument by referring to the iSCSI PDU de-encapsulation process, where the iSCSI PDU the header is being processed by the various protocol processors, including Philbrick's processor 408 or by the HBA controller in the storage network devices. The Examiner seems to allege that Satran teaches that the iSCSI protocol are in fact two separate protocols, namely the TCP/IP protocol (the alleged second traffic type), and the SCSI protocol (the alleged first traffic type).

The Applicant respectfully disagrees and refers the Examiner to the disclosure of iSCSI by Satran, which is incorporated by reference in Philrbick's ¶0065. Specifically, Satran in section 1.2 discloses that "the **iSCSI protocol is a mapping** of the **SCSI remote procedure invocation model over the TCP protocol**." In the same section, Satran also teaches such iSCSI communication protocol is sent in the form of a communication message, referred to the term "iSCSI protocol data unit" (iSCSI PDU). In other words, Satran clearly teaches that the iSCSI is a protocol that maps the SCSI protocol over the TCP protocol, and such protocol is communicated through a message type, which is also known as a **iSCSI PDU message**. Therefore, the Examiner's argument that the iSCSI PDU has two separate and distinct network traffics is contrary to the disclosure of Satran.

Furthermore, the Applicant points out the Examiner seems to ignore the fact that the processing of the iSCSI PDU messages headers (i.e., the de-encapsulation process) by various processors takes place only after the iSCSI PDUs has been

transported via the network link, the fabric and received by the Ethernet connector . In other words, the iSCSI PDU messages are still considered as a single traffic type, having a single connection source and destination address before being processed.

Based on the above rationale, the Applicant maintains the argument in the July 24, 2008 reply to the Office Action that the iSCI traffic is of a single traffic type, and not two separate types. Therefore, Philbrick does not disclose or suggest the claimed "a single Ethernet connector **for handling a plurality of different types of network traffic transported via the single fabric**," as recited in the Applicant's claim 18.

Furthermore, regarding the rejection of claim 18, the Applicant further submits that Philbrick does not disclose or suggest "a single Ethernet connector for handling a plurality of different types of network traffic transported via a single fabric, ...**the single fabric is coupled to a plurality of servers**," as recited by the Applicant in claim 18. The Examiner equates Philbrick's single wire connecting between the MAC 424 and the processor 408 inside the INIC 400 to the claimed "single fabric". The Applicant respectfully disagrees, and points out that not only the MAC 424 is not a "single **Ethernet connector**", but also Philbrick discloses that the alleged single fabric (single wire) **connects between the MAC 424 and the processor 408 inside the INIC 400**, therefore, Philbrick's alleged single fabric does not read on "**the single fabric is coupled to a plurality of servers**," as recited by the Applicant in claim 18.

Therefore, based on the foregoing rationale, the Applicant respectfully maintains that Philbrick does not anticipate the Applicant's limitation of "a **single integrated convergent network controller chip**, and a **single Ethernet connector for handling a plurality of different types of network traffic transported via a single fabric,** said single Ethernet connector is coupled to **the single integrated convergent network controller chip ... operable to concurrently handle a plurality of different types of traffic,... the single fabric is coupled to a plurality of servers**" as recited by the Applicant in claim 18. Claim 18 should therefore be allowable based on the above rationale.

Likewise, independent claims 1, 26, 33, 36 and 39 are similar in many respects to claim 18, are also submitted to be allowable based on the same rationale of claim 18. Furthermore, The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of independent claim 18 should such a need arise.

A(2) Dependent Claims 20 and 22-25, 27-29, 31-32, 37-38 and 40-41

Based on at least the foregoing, the Applicant believes the rejection of independent claims 18, 26, 36 and 39 under 35 U.S.C. § 102(e) as being anticipated by Philbrick has been overcome and requests that the rejection be withdrawn. Additionally, claims 20 and 22-25, 27-29, 31-32, 37-38 and 40-41 depend directly or indirectly from

independent claims 18, 26, 36 and 39 and are, consequently, also respectfully submitted to be allowable.

In addition, with regard to the rejection of claim 25, the Examiner is referred to the same rationale in Section I, that **the iSCSI traffic is a single type of traffic comprising iSCSI PDU messages**. Philbrick does not disclose the claimed limitation of other traffic types, i.e. the IPC traffic or the cluster traffic, that are concurrently handled by the Ethernet connector and the integrated chip. Claim 25 is therefore allowable. Likewise, claims 38 and 41 are allowable for the same rationale as in claim 25.

The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of dependent claims 20 and 22-25, 27-29, 31-32, 37-38 and 40-41 should such a need arise.

III. REJECTION UNDER 35 U.S.C. § 103

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure ("MPEP") states the following:

> "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the teaching. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

See MPEP at § 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination," and that "although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be *a suggestion or motivation in the reference* to do so'" (citing In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)). Moreover, MPEP § 2143.01 also states that the level of ordinary skill in the art cannot be relied upon to provide the suggestion...," citing Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 50 USPQ 2d 1161 (Fed. Cir. 1999). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness.

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

A. The Proposed Combination of AAPA and Philbrick Does Not Render Claims 1-15 Unpatentable

The Applicant turns to the rejection of claims 1-15 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Philbrick.

A(1). Independent Claim 1

With regard to the final rejection of independent claim 1 under 35 U.S.C. § 103(a), the Applicant submits that the combination of AAPA and Philbrick does not disclose or suggest at least the limitation of 'the first server comprising **a first single integrated convergent network controller chip**,... the second server comprising **a second single integrated convergent network controller chip**,... the third server comprising **a third single integrated convergent network controller chip**," as recited in claim 1 by the Applicant.

The Examiner is referred to Figs. 1 and 4 of AAPA, and the Applicant points out that AAPA discloses that each of the first, second and third server **uses multiple controller chips** instead of using a single integrated convergent network controller chip in each of the servers. Philbrick does not overcome the above deficiencies of AAPA.

In addition, with regard to the rejection of claim 1, the Applicant submits that the combination of AAPA and Philbrick does not disclose or suggest at least the limitation of "a second tier coupled to the first tier via a single fabric coupled to a single connector,... a third tier coupled to the second tier via the single fabric coupled to the single connector," as recited in claim 1 by the Applicant.

The Examiner is referred to Fig. 1 of AAPA, and the Applicant points out that AAPA discloses that servers 1, 2 and 3 are coupled to each other via a plurality of fabrics, not a single fabric. More specifically, the server Type B is coupled to Type A

and Type C via two fabrics instead of a single fabric. Philbrick does not overcome the above deficiencies of AAPA.

Furthermore, the Applicant submits that the combination of AAPA and Philbrick does not disclose or suggest at least the limitation of "wherein **the first server, the second server and the third server process, respectively via the first single integrated convergent network controller chip, the second single integrated convergent network controller chip and the third single integrated convergent network controller chip, a plurality of different traffic types concurrently over the single fabric** that is coupled to the using single connector," as recited in claim 1 by the Applicant. The Examiner concedes in the Final Office Action that:

> "AAPA does not disclose: wherein at least one of the first server, the second server and the third server handles a plurality of different traffic types over a single fabric."

See the Final Office Action in page 8. The Examiner then turns to Philbrick for support and states the following:

> "However, Philbrick discloses: wherein at least one of the first server, the second server and the third server handles a plurality of different traffic types over a single fabric (fig. 6, a server handles iSCSI and TCP/IP over a single fabric connecting the Ethernet connector 424 and processor 408)."

See the Office Action in page 9. The Applicant again refers the Examiner to the same argument above that AAPA and Philbrick do not disclose a first, a second and a third single integrated convergent network controller chips to concurrently process a

plurality of different traffic types, nor do the combination of AAPA and Philbrick discloses a single fabric.

In addition, the Examiner is also referred to the arguments in Section I above, that the iSCSI traffic type is of a single type in the fabric, when received by the single Ethernet connector and by the MAC 424, before being further processed by the processor 408, the host CPU 30 in the protocol stack 38 or by the HBA controller in the network storage devices.

Therefore, the Applicant respectfully maintains that the combination of AAPA and Philbrick does not establish a prima facie case of obviousness to reject the Applicant's claim 1. Claim 1 should therefore be allowable based on the above rationale. The Applicant respectfully requests that the rejection of independent claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Furthermore, The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of independent claim 1 should such a need arise.

A(2) Dependent Claims 2-15

Based on at least the foregoing, the Applicant believes the rejection of the amended independent claim 1 under 35 U.S.C. § 103(a) as being rendered obvious by combining AAPA and Philbrick has been overcome and requests that the rejection be

withdrawn. Additionally, claims 2-15 depend from the amended independent claims 1, and are, consequently, also respectfully submitted to be allowable and requests that the rejection under 35 U.S.C. § 103(a) be withdrawn.

The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of dependent claims 2-15 should such a need arise.

B. The Proposed Combination over Philbrick and Microsoft Does Not Render Claims 33-35, 30 Unpatentable

The Applicant turns to the rejection of claims 33-35, 30 under 35 U.S.C. § 103(a) as being unpatentable over Philbrick as applied to claim 26 above, and further in view of Microsoft.

B (1) Independent Claim 33

With regard to the rejection of independent claim 33 under 35 U.S.C. § 103(a), the Applicant submits that claim 33 and claim 26 are similar in scope and in many respect. The Examiner is referred to the same arguments above in Section 1, that Philbrick does not disclose that the controller MAC 424 is "a layer 2 (L2) connector". In addition, Philbrick also does not disclose "a single integrated convergent network controller chip" to process "a plurality of different types of traffic". Moreover, Philbrick and Satran do not disclose that the iSCSI PDU traffic in the single fabric are **two different types** of traffic, before being processed by the processor 408.

Therefore, the Applicant maintains that Philbrick does not disclose or suggest "said single fabric comprises a single layer 2 (L2) connector coupled to a single integrated convergent network controller chip... concurrently processes a plurality of different types of traffic," as recited in claim 33 by the Applicant. Microsoft does not overcome the limitation deficiency in Philbrick. Accordingly, a prima facie case of obviousness cannot be established by the combination of Philbrick and Microsoft to reject claim 33, therefore claim 33 should be allowable.

The Applicant respectfully requests that the rejection of claim 33 under 35 U.S.C. § 103(a) be withdrawn. Furthermore, the Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of claims 33 should such a need arise.

B(2) Dependent Claims 34-35 and 30

Based on at least the foregoing, the Applicant believes the rejection of the independent claims 26 and 33 have been overcome. Additionally, claims 30 and 34-35 depend from the respective independent claims 26 and 33, and are, consequently, also respectfully submitted to be allowable and requests that the rejection under 35 U.S.C. § 103(a) be withdrawn. The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of dependent claims 30 and 34-35 should such a need arise.

C. The Proposed Combination of AAPA-Philbrick-Microsoft Does Not Render Claims 16 and 17 Unpatentable

The Applicant submits that respective dependent claims 16 and 17 depend directly or indirectly from the respective amended independent claims 1 and 18, and are allowable for at least the same rationale as discussed above for the respective amended independent claims 1 and 18. Accordingly, the Applicant respectfully submits that dependent claims 16 and 17 are also allowable and requests that the rejection under 35 U.S.C. § 103(a) be withdrawn.

The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of dependent claims 16 and 17 should such a need arise.

D. The Philbrick-and What was known in the Art Does Not Render Claims 19 and 21 Unpatentable

The Applicant submits that respective dependent claims 19 and 21 depend directly or indirectly from the respective amended independent claims 1 and 18, and are allowable for at least the same rationale as discussed above for the respective amended independent claims 1 and 18. Accordingly, the Applicant respectfully submits that dependent claims 19 and 21 are also allowable and requests that the rejection under 35 U.S.C. § 103(a) be withdrawn.

Furthermore, the Applicant respectfully requests the Examiner to provide support for the allegation of well known art in rejecting claims 19 and 21, as required by MPEP at § 2142 Specifically, the Examiner is referred to:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

The Applicant reserves the right to argue additional reasons beyond those set forth herein to support the allowability of dependent claims 19 and 21 should such a need arise.

IV. New Claims 42-49

The Applicant has added new claims 42-49. The Applicant points out that support for the above listed new claims may be found at least in paragraphs [0014]-[0016], [0033]-[0040] and in Figs. 6, 7 and 9. Claims 42-45, and 46-49 depend directly or indirectly from claims 1 and 26 respectively, also respectfully submitted to be allowable.

CONCLUSION

Based on at least the foregoing, the Applicant believes that all pending claims 1-2, 4-21 and 25-49 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Patent Agent at (312) 775-8093.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Notice of Allowability is courteously solicited.

Respectfully submitted,

Date: December 12, 2008

/ Frankie W. Wong /

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